**Verilog code to implement BCD to Excess-3 using Behavioral stlye**

**Design Code:**

module fa(input a,b,c, output s,cy);

    assign s = a^b^c;

    assign cy = a&b | b&c | a&c;

endmodule

module adder(input [7:0] a,b, output [7:0] s, output cy);

    wire [8:0] x;

    genvar i;

    assign x[0] = 1'b0;

    generate for(i = 0; i < 8; i = i+1) begin:add

        fa dut(a[i],b[i],x[i],s[i],x[i+1]);

    end

     endgenerate

    assign cy = x[8];

endmodule

**Test Bench:**

module tb();

    reg [7:0] a,b;

    wire [7:0] s;

    wire cy;

    adder dut(a,b,s,cy);

    initial begin

        repeat(10) begin

            a = $random;

            b = $random;

            #1;

            if ({cy,s} == a+b) $display("SUCCESS");

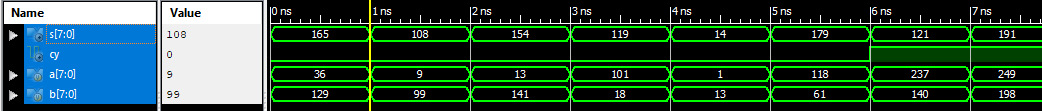
            else $display("FAILURE");

        end

    end

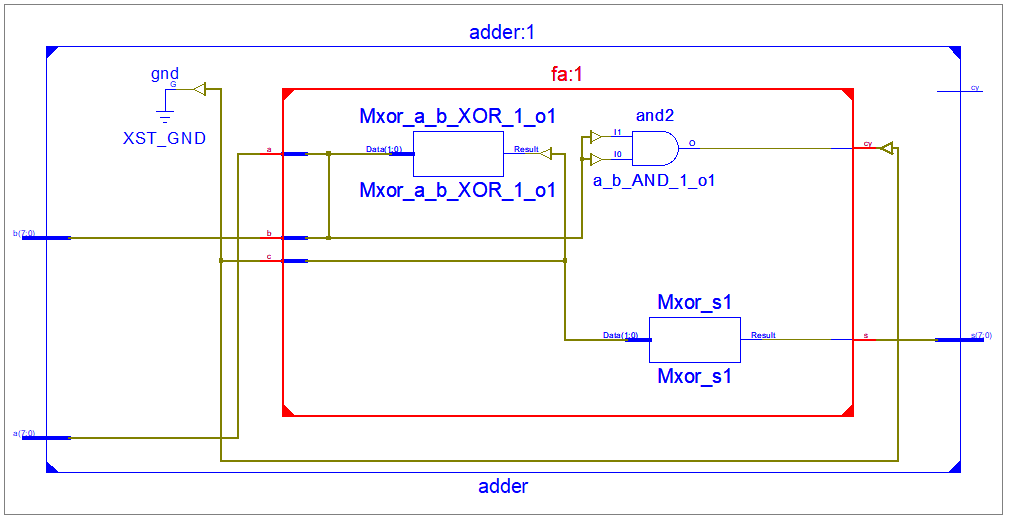
endmodule

**Simulation Result:**

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**RTL Diagram:**

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